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VECTOR-MATRIX MULTIPLICATION IN TERNARY OPTICAL COMPUTER

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Abstract. This paper proposes a new means to complete the optical vector-matrix multiplication (OVMM). The OVMM is implemented on a novel optical computing architecture, ternary optical computer (TOC) by using modified signed-digit (MSD) number system. In addition, this study realizes optical addition in three steps, independent of the length of the operands, by four transformations in MSD, and discuses the multiplication of two MSD numbers in detail. A preliminary experimentation about the OVMM is performed on TOC. It illustrates that the proposed method for OVMM is feasible and correct.

Key words. parallel, modified signed-digit, no-carry addition, basic operating unit, partial sum

1. Introduction

Optical vector-matrix multiplication (OVMM) was proposed by Lee et al. in 1970[1]. Since then, many optical means have been put forward to implement OVMM[2-23]. However, most of them are analog computing systems only using light intensity, so their apparatus and experimental conditions are very sensitive to noise. In order to improve the accuracy, some algorithms and technologies were applied to OVMM, such as digital multiplication by analog convolution[7, 12], twos complement arithmetic[7, 11], error-correcting codes [6, 9], time-and-space integrating[12, 23], and digital partitioning[9]. In 2009, Li et al realized binary OVMM in ternary optical computer(TOC)[22]. However, Li's work was short of application because every element in the matrix and vector was only one bit.

On the other hand, numerical redundant representations have been used in no-carry addition or other arithmetic operations in the past several decades. It is most worth to mention that in those redundant representations, the modified signed-digit (MSD) number system is often used in optical computing[24, 25, 26]. The MSD, using three digits, -1, 0, and 1 with radix-2, has been proved to be well suited for realizing no-carry addition and other arithmetic operations. In the number system, the carry propagation occurs only between the neighboring positions in the addition operation and the results can be obtained through three logical steps by four logic operations. Therefore MSD is a parallel computing means. This paper will propose a method for immplementing OVMM via MSD number system in TOC.

The remainder is organized as follows. Section 2 discusses the main technological foundations. Section 3 is the theory of the proposed method. Section 4 gives an experiment to verify the method. And the last section is a summary.

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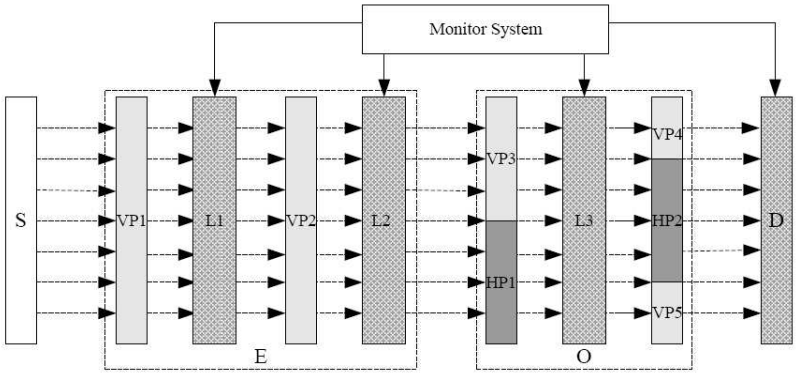

FIGURE 1. Architecture of the optical part in TOC.

2. Foundations

2.1. Optical Core of TOC Experimental System. The principle and architecture of TOC was proposed by Jin[28, 29]. In TOC, three steady states of light, no intensity light (NIL), horizontal polarization light (HPL) and vertical polarization light (VPL), are used to represent tri-valued information. In 2007 an experimental TOC system was built in Shanghai University. In the experimental system there is an optical core made up of a light source, 5 pieces of vertical polarizer (VP1, VP2, VP3, VP4 and VP5), 2 pieces of horizontal polarizer (HP1 and HP2), 3 monochromatic liquid crystal arrays (L1, L2 and L3) and 1 photoreceptor array (D), shown in Figure 1. The core can be divided functionally into four components,a light source (S) , an encoder (E, including VP1, L1, VP2 and L2), a processor (O, containing VP3, HP1, L3, VP4, HP2, VP5 and L3), and a decoder (D).

The optical processor (O) has four partitions from top to down, which are called respectively VV, VH, HV, and HH, shown in Figure 1. Each partition has the same structure: two pieces of polarizer holding a liquid crystal array in between, seeming like a sandwich. If the partition has a vertical polarizer in the front and a horizontal one in the back, it is called a VH partition. Other namings of the partitions follow similar rules.

2.2. Decrease-Radix Design Principle. In 2007, reference[30] proposed the decrease-radix design principle (DRDP). With this principle, each of n^{n^2} n-valued arithmetic unit without carry or borrow can be constructed by combining several simplest hardware units if there exists a special one (it is called D state in our work) included in the n physical states used to represent information. The sort of the simplest hardware units is $n^2\,(n-1)$, and they are called the basic operating-units(BOUs).

Applying the DRDP to TOC, we can get the results as follows:

- Any two-input tri-valued logic processor can be reconfigured by no more than 6 BOUs at any moment. And the total of the two-input tri-valued logic processors is 19683.
- There are 18 kinds of BOUs in total.
- Each BOU is made of a liquid crystal pixel and a piece of polarizer on each side of it(see "O" in Figure 1).